MICRO COMPARITOR
INPUT / OUTPUT ELECTRONIC CHARACTERISTICS
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Fig #1 shows circuit(s) of the Sense, Credit and Tilt outputs. The pull-up resistors for the three outputs are optional, depending on the printed circuit board installed in the mechanism.

Fig #2 shows the circuit of the INHIBIT CONTROL (INPUT). This circuit is ideally controlled by an "OPEN" and "GROUND". It also works with logic voltage levels of "5VDC" and "GROUND"

Fig #3 on page 2 of this document show an oscilloscope shot of the Sense and Credit pulses during a three coin fast feed using the 0950-000081 firmware.
Each Sense pulse is 17mS +/- 1mS in length. The minimum amount of time between each Sense pulse is 13mS +/- 1mS. The time from the beginning of the Sense pulse and the beginning of the next Sense pulse is call the Sense Period. By adding the two times together you get a Minimum Sense Period of 30mS +/- 1mS.
The Credit pulse length is 13mS in length. The minimum time between Credit pulses is 17mS. The minimum Credit Period is 30mS +/- 1mS.

On page 2 of this document are generic timing specifications for the MC-2 firmware. The pulse lengths, time between pulses and Inhibit logic levels are different from one firmware to another, depending on the machine manufacturer's requirements.

Fig #1
Output Circuit(s)

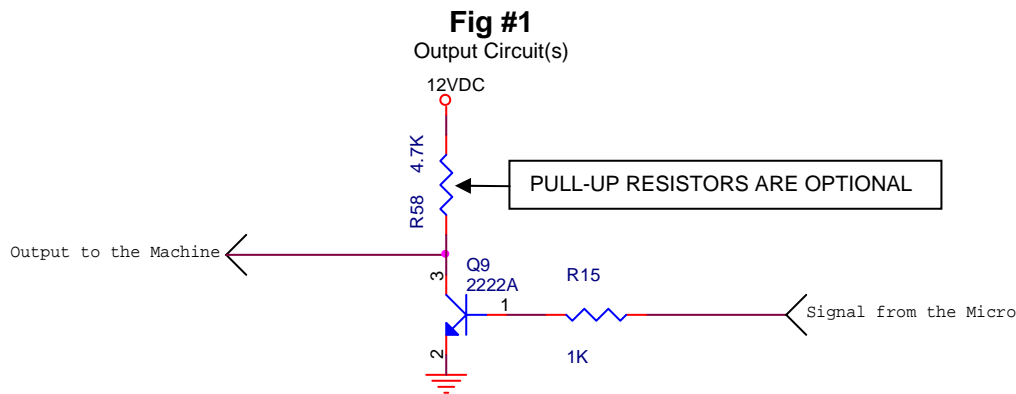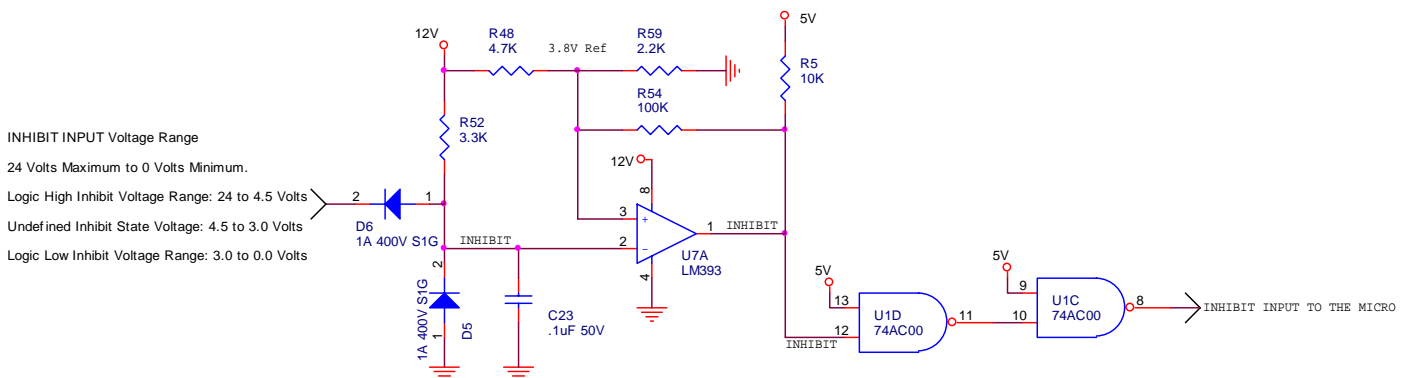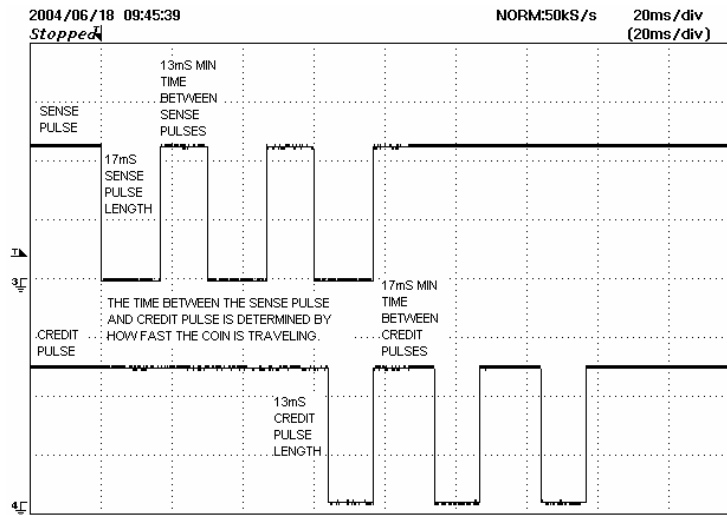
PULL-UP RESISTORS ARE OPTIONAL

Fig #2
Inhibit Control (Input)

INHIBIT INPUT Voltage Range

24 Volts Maximum to 0 Volts Minimum.

Logic High Inhibit Voltage Range: 24 to 4.5 Volts

Undefined Inhibit State Voltage: 4.5 to 3.0 Volts

Logic Low Inhibit Voltage Range: 3.0 to 0.0 Volts

Fig #3
Output pulse length and timing example using 0950-000081 firmware

2004/06/18 09:45:39   NORM:50kS/s   20ms/div
Stopped   (20ms/div)

SENSE PULSE

13mS MIN TIME BETWEEN SENSE PULSES

17mS SENSE PULSE LENGTH

THE TIME BETWEEN THE SENSE PULSE AND CREDIT PULSE IS DETERMINED BY HOW FAST THE COIN IS TRAVELING.

17mS MIN TIME BETWEEN CREDIT PULSES

CREDIT PULSE

13mS CREDIT PULSE LENGTH

MC-2 COIN MECHANISM
Generic
SOFTWARE OPERATING PARAMETERS

Power Up Delay Timer =20 Milliseconds
Starts when power is first applied to Microcontroller and Instructions are being executed.
The unit remains inactive for this time.
System Test Delay = 70 Milliseconds

Inhibit = LOW or HIGH depending on firmware
Minimum Inhibit Input = 3 Milliseconds
Minimum Inhibit Timer = 50 Milliseconds
After an Inhibit signal is detected the unit will remain Inhibited for this minimum
time period regardless of the state of the Inhibit Input.

Sense Pulse Length = See spec sheet
Sense Pulse Period = See spec sheet
Minimum Pulse off Time = 13 Milliseconds Min.

Maximum Exit Optic Blockage Timer = 1.5 Seconds
Any Exit Optic Signal longer than this will cause a TILT.

Credit Pulse Length =See spec sheet
Credit Pulse Period =See spec sheet
Minmimum Pulse off Time = 17 Milliseconds Min.

Minimum Tilt Pulse Length = 13 Milliseconds
When a Tilt is detected, the mechanism is disabled for 13 sec.

TILT CONDITIONS
Excessive NULL
Excessive Exit Optic Blockage
When more than 1 non-sensed coin passes the Exit Optics (Intelligent Slug Tilt)
When the Exit Optics Detect a Reverse Coin. (Stringing)
When the Pending Coin Timer counts down to Zero (Slow Moving Coin)